Patent claims

1. A test device for testing integrated circuits, in particular dynamic AD converters, the test device (3; 4) comprising the following features:
- a precision signal generator (201), which is intended for generating a test signal and which is connected via a respective connecting line (306; 409) to a respective input contact (211; 221; 231) intended for connection to an input of an integrated circuit,
- at least one reference signal generator (301; 401, 411) intended for generating a reference signal,
- at least one comparator unit (303; 403, 413; 501, 511, 521) is provided for a respective input contact (211, 221, 231), said comparator unit being operable in a test mode and being constructed such that the test signal can be compared with the reference signal and that the precision signal generator (201) can be turned off by the comparator unit (303; 403, 413; 501, 511, 521) if the test signal exceeds or falls below the reference signal.

2. The test device according to claim 1, wherein two reference signal generators (401, 411) are provided, the first reference signal generator (401) being intended for generating a lower reference signal and the second reference signal generator (411) being intended for generating an upper reference signal, a first comparator unit (403; 501, 511, 521), which id connectable to the first reference signal generator (401), and a second comparator unit (413; 501, 511, 521), which is connectable to the second reference

signal generator (411), being provided for each input contact (211, 221, 231).

3. The test device according to claim 1 or 2, wherein
the reference signal generator (301) or the first and second reference signal generators (401, 411) in each case has/have a calibration line (307; 406, 416) and a reference line (308; 407, 417), the/each comparator unit (303; 403, 413; 501, 511, 521) being connected to the calibration line (307; 406, 416) and to the reference line (308; 407, 417) of the relevant reference signal generator (301; 401, 411), each comparator unit (303; 403, 413; 501, 511, 521) having a calibration unit (303; 403, 413), and the comparator unit (303; 403, 413; 501, 511, 521) also being operable in a calibration mode constructed such that the switching properties of the comparator unit (303; 403, 413; 501, 511, 521) being adjustable by the calibration unit (303; 403, 413) by means of the signal values of the calibration line (307; 406, 416) which are present at the comparator unit (303; 403, 413; 501, 511, 521).and by means of the reference line (308; 407, 417)

4. The test device according to claim 3, wherein
the comparator unit (303) or the comparator units (403; 413; 501, 511, 521) are switchable back and forth between the test mode and the calibration mode.

5. The test device according to one of claims 1-4, wherein
the comparator unit(s) (303; 403, 413; 501, 511, 521) in each case has/have a comparator (302; 402, 412).

6. The test device according to claim 5, wherein

a respective comparator (302; 402, 412) has two inputs and an output, the first input of each comparator (302; 402, 412) being connected to the reference line (308; 407, 417) of the relevant reference signal generator (301; 401, 411), the second input of each comparator (302; 402, 412) being connectable to the calibration line (307; 406, 416) of the relevant reference signal generator (301; 401, 411) and to the connecting line of its input contact (211, 221, 231) the output of each comparator being connectable to its calibration unit (303; 403, 413) and to the precision signal generator (201) and the switching properties of the calibration unit (303; 403, 413) being adjustable by the comparator (302; 402, 412).

7. The test device according to one of claims 1-6, wherein
a decision logic unit (531) is provided, which is connected to the comparator units (501, 511, 521) and which is constructed such that control signals are generated for the precision signal generator (201) from the output signals of the comparator units (501, 511, 521).

8. The test device according to one of claims 1-7, wherein
a respective output contact (212, 222, 232) intended for connection to an output of an integrated circuit is provided for each input contact (211, 221, 231), said output contact being connected to an output line.

9. The test device according to claim 8, wherein
a respective validation signal line (504, 514, 524) leads from each comparator unit (501, 511, 521) to the relevant output line.

10. The test device according to one of claims 1-9, wherein
the test device (3; 4) is monolithically integrated on an integrated circuit.

11. A load board for receiving at least one needle card (108) for testing integrated circuits and/or having at least one test receptacle for testing integrated circuits and/or for connecting a handler to a tester (1) of integrated circuits, the load board having a test device (3; 4) according to one of claims 1-9.

12. A tester for testing integrated circuits comprising the following features:

- the tester (105) has a plurality of instruments for generating signals or data streams, and a plurality of measuring sensors, in particular for currents and voltages,
- the tester (105) has a load board which is provided for receiving at least one needle card (108) for testing integrated circuits and/or for connecting a handler to a tester of integrated circuits and/or which is equipped with at least one test receptacle for testing integrated circuits,
- the tester (105) has a test device (3; 4) as claimed in one of claims 1-10, the precision signal generator (201) and the reference signal generator (301) or the reference signal generators (401, 411) being formed on the tester (105), and the comparator unit(s) (303; 403, 413; 501, 511, 521) with the calibration unit (303) / with the calibration units (403, 413) being arranged on the load board, adjacent to the input contacts (211, 221, 231) for the integrated circuits.

13. A method for parallel testing of integrated circuits comprising the following steps of:

a) providing a tester (105) having a load board which is provided for receiving a plurality of needle cards (108) for testing integrated circuits and/or for connecting a handler to a tester (105) of integrated circuits and/or which is equipped with a plurality of test receptacles for testing integrated circuits,

b) populating the load board with a plurality of integrated circuits, a precision signal generator (201), at least one reference signal generator (301; 401, 411) and, for each integrated circuit, a respective comparator unit (303; 403, 413; 501, 511, 521) being provided,

c) carrying out a test mode having the following steps:

c1) generation of a test signal by a precision signal generator (201) and application of the test signal to the integrated circuits,

c2) generation of at least one reference signal by the reference signal generator (301)/by the reference signal generators (301; 401, 411) and application of the reference signal/reference signals to the comparator units (303; 403, 413; 501, 511, 521),

c3) comparison of the test signal with the respective reference signal by the comparator units (303; 403, 413; 501, 511, 521),

c4) turning-off of the precision signal generator (201) by one of the comparator units (303; 403, 413; 501, 511, 521) if the test signal exceeds or falls below the reference signal.

14. The method according to claim 13,

wherein

the provided reference signal generator (301) or the first and second reference signal generators (401, 411)

in each case has or have a calibration line (307; 406, 416) and a reference line (308; 407, 417), in which case, before or after the test mode is carried out, a calibration mode having the following steps is carried out:

d) connection of each comparator unit (303; 403, 413; 501, 511, 521) to the calibration line (307, 406, 416) and to the reference line (308; 407, 417) of the relevant reference signal generator (301; 401, 411),

e) setting of the switching properties of the comparator units (303; 403, 413; 501, 511, 521) by means of the signal values of the calibration (307; 406, 416) and the reference line (308; 407, 417) which are present at the relevant comparator units (303; 403, 413; 501, 511, 521).

15. The method according to claim 13 or 14, wherein the method steps are carried out by means of a test device of one of claims 1-10, by means of a load board as claimed in claim 11 or by means of a tester (1) as claimed in claim 12.

16. A computer program for executing a method for parallel testing of integrated circuits, which is constructed such that method steps c)-e) in accordance with one of claims 13-15 can be executed.

17. The computer program according to claim 16, which is contained on a storage medium, in particular in a computer memory or in a random access memory.

18. The computer program according to claim 16, which is transmitted on an electrical carrier signal.

19. A data carrier having a computer program as claimed in claim 16.

20. A method in which a computer program according to claim 16 is downloaded from an electronic data network, such as from the Internet, for example, onto a computer connected to the data network.